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HIT 2 482-06

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

T. WATANABE et al

Serial No. 09/739,758 Group Art Unit: 2121

Filed: December 20, 2000 Examiner: J. Hirl

For: NEURAL NETWORK PROCESSING SYSTEM USING SEMICONDUCTOR MEMORIES

RESPONSE

Commissioner for Patents
Mail Stop AF
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Alexandria, VA 22313-1450

Sir:

In response to the Final Rejection mailed on September 26, 2003, and further to the Notice of Appeal and one-month Extension of Time filed on January 26, 2004, Applicants respond as follows.

Personal Interview

Applicants wish to thank the Examiner for conducting a personal interview with the undersigned on January 29, 2004. The following incorporates the substance of that which was discussed during the interview. These arguments are being formally made of record so that the application may be placed in condition for allowance.

Rejection under 35 USC §112, first paragraph.

Claims 25-27, 29, 33, 34 and 36 stand rejected under 35 USC 112, first paragraph. The Examiner alleges that the specification is silent with respect to a "first node" and a "second node". Applicants position as set forth in the interview is as follows.

The specification is not silent on "first mode" and "second mode". This first mode corresponds to the memory mode while the second mode corresponds to the arithmetic mode. The Examiner's attention is directed to pages 30-37 and the description with respect to Figs. 11, 13(a) and 13(b).

On page 30, lines 17-23, it is clearly stated that there is a memory mode and an arithmetic mode. The MOS transistor described in claim 25 is supported in Fig. 11 as T3 and its relation with the first and second mode is supported in Figs. 13(a) and 13(b). ϕ_N turns off T3 in the memory mode as shown in Fig. 13(a) and turns T3 on in the arithmetic mode as shown in Fig. 13(b). While the specification may not specifically use the words "first" and "second" to describe each mode, such is not necessary under current U.S. patent practice. The first and second modes are clearly described in the claims to correspond to the memory mode and the arithmetic mode.

For example, claim 25 specifies that "in said first mode said read operation and said write operation to said memory array are performed." This corresponds to the memory mode. Claim 25 also specifies that "in said second mode information is read from said memory array to said processing circuit." This corresponds to the arithmetic mode. Therefore, both modes are clearly defined in both the specification and the claims.

Rejection under 35 USC §102

Claims 25-37 stand rejected under 35 USC 102(e) as being anticipated by Mashiko (U.S. Patent No. 4,988,891). This rejection is traversed as follows.

A substantial portion of the rejection based upon Mashiko seems to be premised upon the Examiner's position that Applicants' specification does not support a "first mode" and "second mode". However, as described above in the section under 35 USC 112, ample support for this terminology has been provided. Clearly, Mashiko cannot perform a memory function and a logic function independently as in the present invention since Mashiko does not have three separate busses, as described, for example, in claim 29. In addition, Mashiko cannot perform the functions corresponding to the first mode and the second mode in the manner recited in claim 25.

In light of the clarifications made with respect to Applicants' invention during the interview, it is submitted that the rejection under this section be withdrawn. The Examiner is hereby invited to contact the undersigned by telephone if any further clarification is needed.

Labeling Figs. 1-25 as Prior Art

Figs. 1-25 are not prior art since this application is a continuation of an application granted as U.S. Patent No. 6,205,556. Therefore, this application and U.S. Patent No. 6,205,556 have identical effective filing dates, as such, one cannot be prior art to the other.

IDS

Applicants submit that the IDS filed along with the application on December 20, 2000 properly referenced the parent application, serial no. 09/198,658. There is no obligation to identify the parent application on the PTO-1449 forms themselves. It is submitted that the cover sheet of the Information Disclosure Statement can identify the parent application, to inform the patent office of the relevance of the documents cited in the PTO-1449 forms and their source. In addition, according to 37 CFR 1.98(d), copies of documents that were previously submitted to the Office in an earlier

application do not need to be resubmitted as long as the earlier application is properly identified and the Information Disclosure Statement submitted in the earlier application complies with 37 CFR 1.98 (a)-(c). It is submitted that these requirements have been satisfied.

Nevertheless, as a courtesy to the Examiner, and in response to a request by the Examiner, copies of all of these documents are being resubmitted at this time for the Examiner's convenience. It is requested that the attached copies of the PTO-1449 Forms be initialed, signed and returned along with the next communication from the Patent Office.

Conclusion

In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is in condition for allowance. Accordingly, reconsideration and reexamination are respectfully requested.

Respectfully submitted,

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